Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (currently amended) An apparatus, comprising:

a semiconductor substrate;

a first conducting layer in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal, the base layer metal comprising Cu;

a diffusion barrier in contact with the first conducting layer;

a wetting layer on top of the diffusion barrier; and

a bump layer on top of the wetting layer, the bump layer comprising Sn, wherein the ~~Sn~~ bump layer is an electroplated bump layer ~~being electroplated~~, and wherein the diffusion barrier is configured ~~being formed~~ to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus.

2. (currently amended) The apparatus of Claim 1, wherein the diffusion barrier is ~~an electroless diffusion barrier~~ configured to suppress whisker-type formation in the bump layer.

3. (original) The apparatus of Claim 1, further comprising a solder layer positioned between the bump layer and a die package, wherein the solder layer comprises Sn.

4. (original) The apparatus of Claim 1, wherein the base layer metal comprises an adhesion layer and a seed layer, wherein the adhesion layer comprises one of Ti, TiN, and TiSiN, and the seed layer comprises one of Ni, NiV, and Co.

5. (original) The apparatus of Claim 4, wherein the base layer metal further comprises a metal layer positioned between the adhesion layer and the seed layer, wherein the metal layer comprises Al.

6. (currently amended) The apparatus of Claim 1, wherein the diffusion barrier comprises one of ~~CoBP, CoWP, CoWB, CoWBP,~~ NiBP, NiWP, NiWB, and NiWBP, wherein the bump layer further comprises a Sn alloy, the Sn alloy comprising one of 0.7Cu, Bi, Sb, and 3.5Ag, ~~wherein the Sn bump layer being electroplated~~ and wherein the bump layer is further configured to prevent low temperature phase transition of Sn from alpha Sn into beta Sn.

7. (currently amended) The apparatus of Claim 1, wherein the wetting layer comprises one of CoB~~, NiB,~~ and NiP, wherein

the diffusion barrier is further configured to reduce bump layer delamination.

8. (currently amended) The apparatus of Claim 1, wherein the apparatus further comprises another ~~sputtered~~ base layer metal~~, wherein the diffusion barrier is further configured to reduce electromigration related to CuSn intermetallic formation~~.

9. (currently amended) An apparatus comprising:

a base layer metal on a semiconductor substrate, the base layer metal comprising Cu;

a bump on top of the base layer metal, the bump comprising an electroplated Cu layer;

a diffusion barrier in contact with the bump;

a wetting layer on top of the diffusion barrier; and

a solder layer contacting the bump, the solder layer comprising Sn, wherein the diffusion barrier is ~~being further~~ configured to prevent the diffusion of Cu and Sn through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus.

10. (currently amended) The apparatus of Claim 9, wherein the diffusion barrier ~~comprises an electroless diffusion layer~~ is configured to suppress whisker-type formation in the bump.

11. (currently amended) The apparatus of Claim 9, wherein the base layer metal comprises an adhesion layer and a seed layer, wherein ~~the adhesion layer comprises one of Ti, TiN, and TiSiN, and~~ the seed layer comprises one of Ni~~, NiV,~~ and Co.

12. (currently amended) The apparatus of Claim 10, wherein the base layer metal further comprises a metal layer positioned between the adhesion layer and the seed layer, wherein the metal layer comprises Al~~, wherein the diffusion barrier is configured to suppress a whisker type formation in the bump~~.

13. (currently amended) An apparatus comprising:

a base layer metal on a semiconductor substrate, the base layer metal comprising Cu;

a bump on top of the base layer metal, the bump comprising an electroplated Cu layer;

a diffusion barrier in contact with the bump;

a wetting layer on top of the diffusion barrier; and

a solder layer on top of the wetting layer, the solder layer comprising Sn, wherein the diffusion barrier is ~~being further~~ configured to prevent the diffusion of Cu and Sn through the diffusion barrier and to prevent CuSn intermetallic formation in the apparatus, and wherein the base layer metal

further contacts the diffusion barrier to physically isolate the bump from the solder layer.

14. (currently amended) The apparatus of claim 9, wherein the diffusion barrier comprises one of ~~CoBP, CoWP, CoWB, CoWBP,~~ NiBP, NiWP, NiWB, and NiWBP, wherein the wetting layer comprises one of CoB, ~~NiB,~~ and NiP.

15. (withdrawn) A method comprising:

performing passivation with SiN and polyimide;

depositing a base layer metal;

depositing a photoresist layer;

forming a diffusion barrier, the diffusion barrier being adapted to prevent intermixing of Cu and Sn between different layers;

forming a wetting layer on top of the diffusion barrier;

forming a bump layer;

removing the photoresist layer; and

etching the base layer metal.

16. (withdrawn) The method of Claim 15, wherein the depositing the base layer metal comprises one of a plasma vapor deposition (PVD), a chemical vapor deposition (CVD), and an

atomic layer deposition (ALD), wherein the diffusion barrier comprises an electroless diffusion barrier.

17. (withdrawn) The method of Claim 16, wherein the base layer metal comprises an adhesion layer and a seed layer, wherein the adhesion layer comprises one of Ti, TiN, and TiSiN, and the seed layer comprises one of Ni, NiV, and Co, wherein the electroless diffusion barrier is further adapted to reduce bump layer delamination.

18. (withdrawn) The method of Claim 17, wherein depositing the base layer metal comprises depositing a metal layer positioned between the adhesion layer and the seed layer, wherein the base layer metal further comprises one or more electrical interconnects..

19. (withdrawn) The method of Claim 18, wherein the metal layer comprises Al, wherein the photoresist layer is adapted for patterning, wherein the electroless diffusion barrier is further adapted to reduce electromigration related to CuSn intermetallic formation.

20. (withdrawn) The method of Claim 16, wherein the electroless diffusion barrier comprises one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP.

21. (withdrawn) The method of Claim 16, wherein the bump layer comprises Sn, the Sn being electroplated to prevent low temperature phase transition of Sn from alpha Sn into beta Sn, wherein the Sn being electroplated is further adapted to suppress whisker formation.

22. (withdrawn) The method of Claim 16, wherein the bump layer comprises a Sn alloy, the Sn alloy comprising one of 0.7Cu, Bi, Sb, and 3.5Ag, wherein the Sn alloy is electroplated to prevent low temperature phase transition of Sn from alpha Sn into beta Sn.

23. (withdrawn) The method of Claim 16, further comprising:
forming a solder layer to the bump layer, the solder layer comprising Sn; and
connecting a die package to the solder layer.

24. (withdrawn) A method comprising:
performing passivation with SiN and polyimide;
depositing a base layer metal;

depositing a photoresist layer;

forming a Cu layer, the Cu layer being electroplated;

forming an electroless diffusion barrier, the electroless diffusion barrier being positioned between the Cu layer and a Sn layer, the electroless diffusion barrier being adapted to prevent Cu and Sn from diffusing through the electroless diffusion barrier;

forming a wetting layer on top of the electroless diffusion barrier;

removing the photoresist layer; and

etching the base layer metal.

25. (withdrawn) The method of Claim 24, further comprising forming a solder region on top of the wetting layer and the electroless diffusion barrier, wherein the solder region is in contact with a die package, wherein the solder region comprises Sn.

26. (withdrawn) The method of Claim 24, wherein the Sn layer comprises a solder region on top of the electroless diffusion barrier, wherein the solder region is in contact with a die package.

27. (withdrawn) The method of Claim 24, wherein the electroless diffusion barrier comprises one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP.

28. (withdrawn) A method comprising:

performing passivation with SiN and polyimide;

depositing a base layer metal;

depositing a photoresist layer;

forming a bump layer, the bump layer comprising Cu, the Cu bump layer being electroplated;

removing the photoresist layer;

etching the base layer metal;

forming an electroless diffusion barrier layer, the electroless diffusion barrier layer being positioned between the Cu bump layer and a Sn layer, the electroless diffusion barrier layer being adapted to prevent intermixing of Cu and Sn between different layers; and

forming a wetting layer on top of the electroless diffusion barrier layer.

29. (withdrawn) The method of Claim 28, wherein the electroless diffusion barrier layer comprises one of CoBP, CoWP, CoWB, CoWBP, NiBP, NiWP, NiWB, and NiWBP, wherein the base layer metal comprises an adhesion layer and a seed layer, wherein the

adhesion layer comprises one of Ti, TiN, and TiSiN, and the seed layer comprises one of Ni, NiV, and Co.

30. (withdrawn) The method of Claim 28, wherein the base layer metal further physically contacts the electroless diffusion barrier layer, wherein the bump layer comprises an outer surface, wherein the outer surface of the bump layer is physically isolated from contacting a layer comprising Sn.

31. (withdrawn) The method of Claim 28, wherein the Cu bump layer is further adapted to prevent formation of whisker formation, wherein the electroless diffusion barrier layer is further adapted to reduce electromigration related to CuSn intermetallic formation.

32. (currently amended) A system having a circuit board comprising:

one or more components comprising circuitry; and

one or more layers on the circuit board to route at least one signal between components on the circuit board, wherein at least one of the components on the circuit board comprises a die packing interconnect comprising:

a semiconductor substrate;

a first conducting layer in contact with the semiconductor substrate, the first conducting layer comprising a base layer metal, the base layer metal comprising Cu;

a diffusion barrier in contact with the first conducting layer;

a wetting layer on top of the diffusion barrier; and

a bump layer on top of the wetting layer, the bump layer comprising Sn, wherein the ~~Sn~~ bump layer is an electroplated bump layer ~~being electroplated~~, and wherein the diffusion barrier is ~~being~~ configured to prevent Cu and Sn from diffusing through the diffusion barrier and to prevent CuSn intermetallic formation in the die packing interconnect.

33. (original) The system of Claim 32, wherein the one or more components comprise any one of a central processing unit, a memory, and a logic unit.